Remarks

Claims 9-16 are pending in the application and are presented for reconsideration. Claims 1-8 and 17 have been canceled; Claims 8, 15 and 16 have been amended; and claims 10-14 remain in the application unchanged. No new matter has been added.

Claim Rejections

Claims 4-7 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-2, 7-8 and 15-17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JP 5-37305.

Claims 1-4, 6-8 and 15-17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Chalasani (U.S. Pat. No. 6,864,732).

Claim 9 is rejected under 35 U.S.C. § 102(e) as being anticipated by Markovic et al. (US 2003/0107421).

Claim 5 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Chalasani (U.S. Pat. No. 6,864,732) in view of Shikata et al. (U.S. Pat. No. 4,939,384).

Claims 10-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Markovic et al. (US 2003/0107421).

The Examiner's rejections of the claims are respectfully traversed.

I. Rejection of Claims Under 35 U.S.C. § 112, Second Paragraph

Claims 4-7 are rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-8 have been canceled; rejection of claims 4-7 under 35 U.S.C. § 112, second paragraph is now moot.

II. Rejections of Claims Under 35 U.S.C. § 102

1. Legal standard for Rejecting Claims Under 35 U.S.C. §102

Under 35 U.S.C. § 102, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros., Inc. v. Union Oil Co.*, 814 F.2d 628 (Fed. Cir.), *cert. denied*, 484 U.S. 827 (1987).

2. Rule 37 CFR 1.131 Affidavit

Pursuant to 37 CFR 1.131, Applicant hereby submits an Affidavit supporting the reduction to practice of the invention before the effective filing date of November 18, 2002 of Chalasani.

Exhibit A of the Affidavit is a copy of a schematic of a circuit using the differential register with slave structure of the invention as described in the patent application that is dated prior to November 18, 2002. Exhibit B of the Affidavit is a copy of the computer generated timestamp of the schematic circuit file that was automatically generated by the computer at the time of the circuit's creation prior to November 18, 2002.

Entry of the accompanying Affidavit is proper to overcome the Chalasani reference since the invention was completed prior to the effective filing date of the Chalasani reference. In view of the Affidavit and accompanying Exhibits, it is therefore submitted that the Chalasani reference is now removed from consideration.

3. Response to Rejections of Claims Under 35 U.S.C. § 102

a. Claims 1-8

Claims 1-8 have been canceled; rejection of these claims is now moot.

b. Claims 9-14

The Examiner cites Markovic as anticipating Applicant's claim 9. In particular, the Examiner states that "Figure 1 shows an input signal (80), a first pass gate (20), a master clock signal (CN), a first storage node (output of the

transistor 20), a second pass gate (30), a slave clock (CP), a first inverter (120), a third pass gate (bottom transistor of passing gate 30), a second storage node (output of the transistor 30) as called for in claim 9."

Claim 9 recites:

> A circuit, comprising:
> an input conveying an input signal;
> a first pass gate coupled to the input and enabling a first signal in response to the input signal and in response to a master clock signal generating a clock signal;
> a first storage node coupled to the first pass gate and storing the first signal;
> a second pass gate connected to the first storage node and enabling a second signal in response to the first signal stored in the first storage node and in response to a slave clock signal, wherein the slave clock is a compliment to the master clock signal;
> a first inverter coupled to the first storage node and generating a first inverted signal in response to the first signal stored in the first storage node;
> a third pass gate coupled to the first inverter and enabling a third signal in response to the first inverted signal and in response to the slave clock signal; and
> a second storage node coupled to the second pass gate and coupled to the third pass gate, the second storage node storing the second signal and the third signal.

Markovic describes Figure 1 as follows:

> As shown in FIG. 1, one such low-energy master-slave latch pair flip-flop is a transmission-gate based flip-flop (TGFF) 10 where n-MOS-only clocked transistors 20, 30 are used to reduce energy consumption. However, on-path inverters 40, 50, which are interrupted by clock signals "CP" and "CN" 60, 70, respectively, slow down the flip-flop and increase the energy consumed. Also, inverter 90 places a logic level 1 at Q_M 100 when input 80 is at logic level 0 and clock signal "CN" 70 is activated with a logic level 1. *However, feedback inverter 110 cannot invert the logic level 1 at Q_M 100 due to a logic level 0 at clock signal "CP" 60 that disables inverter 110.* Therefore inverter 90 is unnecessarily consuming energy by "pulling-up" the voltage level at Q_M 100. [Markovic, col. 1, paragraph 0003].

Claim 9 has been amended to more particularly point out the Applicant's invention. Specifically, as shown in Applicant's FIGS. 2 and 3, the first storage node (206, 306) is a differential node that stores the signal at the input to storage

cell 306 and its complement at the output of storage cell 306, respectively. The storage cell 306 is therefore physically connected to the second pass gate (210, 310). In Markovic, however, the first storage node (output of transistor 20) is not physically connected to the second pass gate (30). Instead, an inverter (40) that is clocked by "CP" 60 acts as an additional pass gate between the first storage node (output of transistor 20) and the second pass gate (30). The clocking/enabling of the inverter (40) is an important distinction between, as described in Markovic, col. 1, lines 8-13 of paragraph 0003, there exist time states when the second pass gate (30) is not "connected" to the first storage node (output of transistor 20) since the output of inverter (40) does not always reflect the input of the inverter (40). Accordingly, Markovic does not meet the limitation "a second pass gate ***connected*** to the first storage node and enabling a second signal in response to the first signal stored in the first storage node and in response to a slave clock signal, wherein the slave clock is a compliment to the master clock signal" as required by Applicant's amended claim 9.

Since Markovic does not meet each and every limitation of Applicant's claim 1, per *Verdegaal Bros., Inc., supra*, Markovic cannot be used in formulating an anticipation rejection under 35 U.S.C. § 102.

Furthermore, Markovic cannot be used in formulating a 35 U.S.C. § 103 rejection of Applicant's claim 9. It has been established that "[i]f [the cited reference] does in fact teach away from [Applicant's invention], then that finding alone can defeat [an] obviousness claim." (annotation added) *Winner International Royalty Corp. v. Wang*, 53 USPQ2d 1580, 1587 (Fed. Cir. 2000). A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant . . . [or] if it suggests that the line of development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant." *In re Gurley*, 27 F.3d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994). In addition, if when combined, the references "would produce a

seemingly inoperative device," then they teach away from their combination. *Tec Air*, 52 USPQ2d at 1298 (citing *In re Sponnoble*, 405 F.2d 578, 587, 160 USPQ 237, 244 (CCPA 1969)); *See also In re Gordon*, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (finding no suggestion to modify a prior art device where the modification would render the device inoperable for its intended purpose).

Markovic cannot be used in formulating a 35 U.S.C. § 103 rejection of Applicant's claim 9 because to remove the clocked nature of the inverter (40) in Markovic would be to render the circuit inoperable for its intended function, namely as a "low-energy master-slave latch pair flip-flop" (*see* Markovic, column 1, paragraph 4). Markovic admits this in describing the flip-flop architecture 130, shown in FIG. 2 of Markovic. As stated in Markovic at col. 4, paragraph 4, "pull-up transistors of inverters 90, 120 of FIG. 1 are removed, leaving NMOS transistors, to save energy. However, non-interrupted feedback inverters 140, 150 cause excessive short-circuit energy consumption and a longer time delay arising from a contention with the transmission-gates 160, 170." Thus, a removal of the clocked nature of the inverter (40) in Markovic's Figure 1 would render the circuit inoperable for its intended function of providing a low-energy circuit.

In addition, one of the novel advantages of the structure of Applicant's invention is that upon power-up, the outputs of circuit are guaranteed to be complimentary. However, in Markovic, because the inverters 140 and 110 are enabled only when slave signal "CP" 60 is in an enabling state, if both clock signals "CP" 60 and "CN" 70 power up in the same state, then this will not guarantee complementary outputs.

Accordingly, for all of the above reasons, Markovic cannot even be used in formulating a 35 U.S.C. § 103 rejection of Applicant's claim 9.

None of Japanese Patent 5-37305, Chalasani, Markovic, Shikata, or any of the other prior art of record, taken either alone or in any combination, meets each and every limitation of Applicant's claim 9. Per *Verdegaal Bros., Inc., supra*, therefore none of Japanese Patent 5-37305, Chalasani, Markovic, Shikata, or any of the other prior art of record can be used in formulating an

anticipation rejection under 35 U.S.C. § 102. Furthermore, since none of Japanese Patent 5-37305, Chalasani, Markovic, Shikata, or any of the other prior art of record, taken in any combination, teach the essential limitation "a second pass gate *connected* to the first storage node and enabling a second signal in response to the first signal stored in the first storage node and in response to a slave clock signal, wherein the slave clock is a compliment to the master clock signal", Japanese Patent 5-37305, Chalasani, Markovic, Shikata, or any of the other prior art of record, cannot even be combined to formulate an obvious-type rejection under 35 U.S.C. § 103. Accordingly, Applicant respectfully submits that the rejection of claim 9 should be withdrawn and that claim 9 is now in position for allowance.

Claims 10-14 each depend from independent base claim 1 and add further limitations. For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claims 2-10 are likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of claims 2-10 should be withdrawn.

b. Claims 15-16

Amended claim 15 recites:

> A method of operating a differential register, the differential register comprising a first pass gate having a first pass gate data input, a first pass gate enable input, and a first pass gate output; a first storage node coupled to the first pass gate output; a second pass gate having a second pass gate data input connected to the first storage node and the first pass gate output, a second pass gate enable input, and a second pass gate output; a first inverter having a first inverter input connected to the first storage node and the first pass gate output and a first inverter output; a third pass gate having a third pass gate data input coupled to the first inverter output, a third pass gate enable input, and a third pass gate output; an output node, and a complimentary output node, the method comprising the steps of:
>
> receiving a data input signal on the first pass gate data input and a master clock signal on the first pass gate enable input;
>
> conveying the data input signal from the first pass gate data input to the first pass gate data output and storing the data input signal in the first storage node when the master clock signal is in a first master clock signal state;

receiving the stored data input signal on the second pass gate input and a slave clock signal on the second pass gate enable input;

conveying the stored data input signal from the second pass gate data input to the second pass gate data output for storage in the second storage node when the slave clock signal is in a first slave clock signal state, wherein the slave clock signal is a compliment to the master clock signal;

inverting the stored input data signal to generate an inverted stored input data signal;

receiving the inverted stored data input signal on the third pass gate input and the slave clock signal on the third pass gate enable input;

conveying the inverted stored data input signal from the third pass gate data input to the third pass gate data output for storage in the second storage node when the slave clock signal is in the first slave clock signal state; and

on power-up, conveying the stored data input signal stored in the second storage node out of the output node and conveying the inverted stored data input signal stored in the second storage node out of the complimentary output node.

Claim 15 recites limitations similar to Claim 1, including "a second pass gate having a second pass gate data input *connected* to the first storage node and the first pass gate output" and "receiving the stored data input signal on the second pass gate input". For at least the same reasons that Claim 1 is not shown, taught, or disclosed by the cited references, Claim 15 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 15 should be withdrawn.

Claim 16 depends from independent base claim 15 and add further limitations. For at least the same reasons that Claim 15 is not shown, taught, or disclosed by the cited references, Claim 16 is likewise not shown, taught, or disclosed. Thus, Applicant respectfully submits that the rejection of Claim 16 should be withdrawn.

c. Claim 17

Claim 17 has been canceled; rejection of claim 17 is now moot.

Conclusion

In view of the foregoing remarks, it is respectfully submitted that none of the references cited by the Examiner taken alone or in any combination shows, teaches, or discloses the claimed invention, and that Claims 9-16 are in condition for allowance. Reexamination and reconsideration are respectfully requested.

Should the Examiner have any questions regarding this amendment, or should the Examiner believe that it would further prosecution of this application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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